

What is claimed is:

Sheet 7

1.
A power chip resistor comprising:
a first film resistor having a top surface, a bottom surface,
a first end surface, an opposing end surface, a first
side surface, and an opposing side surface;
a second film resistor having a top surface, a bottom
surface, a first end surface, an opposing end surface, a
first side surface, and an opposing side surface, the
second film resistor of approximately the same physical
size as the first film resistor, the second film
resistor of approximately the same orientation as the
first film resistor;
an encapsulant between the top surface of the first film
resistor and the bottom surface of the second film
resistor, separating the first film resistor and the
second film resistor when the resistors are stacked;
a first nickel barrier connecting the first end surface of
the first film resistor and the first end surface of the
second film resistor;
a second nickel barrier connecting the second end surface of
the first film resistor and the second end surface of
the second film resistor.

2.
The power chip resistor of claim 2 wherein the
first film resistor and the second film resistor are thick
film resistors.

3.
The power chip resistor of claim 1 wherein the first
film resistor and the second film resistor further have
ruthenium oxide resistive elements.

4.

The power chip resistor of claim 1 wherein the encapsulant is inert.

5.

The power chip resistor of claim 4 wherein the encapsulant is glass.

6.

The power chip resistor of claim 5 wherein the encapsulant is glass frit.

7.

The power chip resistor of claim 1 further comprising:
a third film resistor having a top surface, a bottom surface, a first end surface, an opposing end surface, a first side surface, and an opposing side surface, the third film resistor of approximately the same physical size as the second film resistor, the third film resistor of approximately the same orientation as the second first film resistor;
a second encapsulant between the top surface of the second film resistor and the bottom surface of the third film resistor, separating the second film resistor and the third film resistor when the resistors are stacked, the first nickel barrier further connecting the first end surface of the third film resistor with the first end surface of the first film resistor and the first end surface of the second film resistor, the second nickel barrier further connecting the second end surface of the third film resistor with the second end surface of the

first film resistor and the second end surface of the second film resistor.

8.

The power chip resistor of claim 7 further comprising:
a fourth film resistor having a top surface, a bottom surface, a first end surface, an opposing end surface, a first side surface, and an opposing side surface, the fourth resistor of approximately the same physical size as the third film resistor, the fourth film resistor of approximately the same orientation as the third film resistor;
a third encapsulant between the top surface of the third film resistor and the bottom surface of the fourth film resistor, separating the third film resistor and the fourth film resistor when the resistors are stacked, the first nickel barrier further connecting the first end surface of the fourth film resistor with the first end surface of the first film resistor and the first end surface of the second film resistor and the first end surface of the third film resistor, the second nickel barrier further connecting the second end surface of the fourth film resistor with the second end surface of the first film resistor and the second end surface of the second film resistor and the second end surface of the third film resistor.

9.

A power chip resistor comprising:
a first thick film resistor having a top surface, a bottom surface, a first end surface, an opposing end surface, a first side surface, and an opposing side surface;

thick film resistor and the second end surface of the second thick film resistor.

17.

The power chip resistor of claim 16 further comprising:
a fourth thick film resistor having a top surface, a bottom surface, a first end surface, an opposing end surface, a first side surface, and an opposing side surface, the fourth resistor of approximately the same physical size as the third thick film resistor, the fourth thick film resistor of approximately the same orientation as the third thick film resistor;
a third encapsulant between the top surface of the third thick film resistor and the bottom surface of the fourth thick film resistor, separating the third thick film resistor and the fourth thick film resistor when the resistors are stacked, the first nickel barrier further connecting the first end surface of the fourth thick film resistor with the first end surface of the first thick film resistor and the first end surface of the second thick film resistor and the first end surface of the third thick film resistor, the second nickel barrier further connecting the second end surface of the fourth thick film resistor with the second end surface of the first thick film resistor and the second end surface of the second thick film resistor and the second end surface of the third thick film resistor.

18.

A stacked chip resistor comprising:
a first chip resistor and a second chip resistor, each chip resistor having a first end cap and a second end cap, each end cap being an electrical terminal, the first

chip resistor and the second chip resistor capable of being aligned and stacked;
a layer of glass for separating the chip resistors, the layer of glass placed between the first chip resistor and the second chip resistor;
a first nickel barrier, the nickel barrier electrically connecting the first end cap of the first chip resistor and the second end cap of the second chip resistor;
a second nickel barrier, the nickel barrier electrically connecting the second end cap of the first chip resistor and the second end cap of the second chip resistor.

19.

The stacked chip resistor of claim 18 wherein the first film resistor and the second film resistor are thick film resistors.

20.

The stacked chip resistor of claim 18 wherein the first film resistor and the second film resistor further have ruthenium oxide resistive elements.

21.

The stacked chip resistor of claim 18 wherein the glass is glass frit.

22.

The stacked chip resistor of claim 18 wherein each end cap is a silver alloy.

23.

The stacked chip resistor of claim 22 wherein each end cap is a silver palladium.

24.

The stacked chip resistor of claim 18 further comprising:

a third chip resistor, the third chip resistor having a first end cap and a second end cap, each end being an electrical terminal, the third chip resistor capable of being aligned and stacked with the first chip resistor and the second chip resistor;

a second layer of glass for separating the second chip resistor and the third chip resistor, the second layer of glass placed between the second chip resistor and the third chip resistor, the first nickel barrier electrically connecting the first end cap of the third chip resistor with the first end cap of the first chip resistor and the first end cap of the second chip resistor, the second nickel barrier electrically connecting the second end cap of the third chip resistor with the second end cap of the first chip resistor and the second end cap of the second chip resistor.

25.

The stacked chip resistor of claim 24 further comprising:

a fourth chip resistor, the fourth chip resistor having a first end cap and a second end cap, each end being an electrical terminal, the fourth chip resistor capable of being aligned and stacked with the first chip resistor, the second chip resistor, and the third chip resistor;

a third layer of glass for separating the third chip resistor and the fourth chip resistor, the third layer of glass placed between the third chip resistor and the fourth chip resistor, the first nickel barrier electrically

connecting the first end cap of the fourth chip resistor with the first end cap of the first chip resistor and the first end cap of the second chip resistor and the first end cap of the third chip resistor, the second nickel barrier electrically connecting the second end cap of the fourth chip resistor with the second end cap of the first chip resistor and the second end cap of the second chip resistor and the second end cap of the third chip resistor.

26.

Sub 26

A method of manufacturing a stacked power chip resistor comprising:
adhering a first chip resistor to a second chip resistor with a glass encapsulant;
connecting a first terminal of the first chip resistor to a first terminal of the second chip resistor with a metal barrier;
connecting a second terminal of the first chip resistor to a second terminal of the second chip resistor with a metal barrier.

27.

The method of claim 26 wherein the metal barrier is a nickel alloy barrier.

28.

The method of claim 26 wherein the metal barrier is nickel

Add 27